Listing of Claims:

1. (Currently Amended) A data processing system, comprising a memory ~~means (SDRAM)~~ device and a plurality of data processors~~ing means (IP)~~ provided for accessing to said memory device~~means (SDRAM)~~, ~~characterized by~~wherein a communication interface ~~means~~ is coupled between said memory device~~means (SDRAM)~~ and said plurality of data processors~~ing means (IP)~~, said communication interface ~~means~~ including a network of nodes ~~(H.sub.11, H.sub.12, H.sub.2)~~ and a memory interface, each node comprising at least one slave port ~~(s)~~ for receiving a memory access request from a data processor~~ing means (IP)~~ or from a previous node and at least one master port ~~(m)~~ for issuing~~issueing~~ a memory access request to a next node or to said memory device~~means (SDRAM)~~ in accordance with the memory access request received at said slave port ~~(s)~~, wherein ~~said at least~~ one or more slave port~~s (s)~~ ~~is~~are connected to a master port ~~(m)~~ of a previous node, wherein one or more slave ports are connected ~~or~~ to one of said data processors, ~~ing means (IP) and~~ wherein ~~said at least~~ one or more master ports ~~(m) is~~are connected to a slave port ~~(s)~~ of a next node, wherein one or more master ports are connected to the memory interface ~~or to said memory means (SDRAM)~~, wherein the memory interface arbitrates access to the memory device, wherein the communication interface is positioned on a single chip, and wherein the memory device is not positioned on the single chip .

2. (Currently Amended) The data processing system according to claim 1, where~~in characterized in that~~ at each node ~~means~~ the number of said slave ports ~~(s)~~ is higher than the number of said master ports ~~(m)~~.

3. (Currently Amended) The data processing system according to claim 1, where~~in characterized in that~~ said network of node~~s means (H.sub.11, H.sub.12, H.sub.2)~~ is hierarchically structured.

4. (Currently Amended) The data processing system according to claim 3,

~~characterized in that~~wherein said networkplurality of nodes ~~means (H.sub.11, H.sub.12, H.sub.2) are~~is arranged in a directed acyclic graph structure.

5. (Currently Amended) The data processing system according to claim 4, ~~characterized in that~~wherein said network ~~plurality~~ of nodes ~~means (H.sub.11, H.sub.12, H.sub.2) are~~is arranged in a tree structure.

6. (Currently Amended) The data processing system according to claim 1, ~~characterized in that~~wherein said network ~~plurality~~ of nodes ~~means (H.sub.11, H.sub.12, H.sub.2)~~ include n groups of nodes ~~means~~ with $n \geq 2$, wherein each of the slave ports ~~(s)~~ of the nodes ~~means (H.sub.11)~~ of a first group is connected to one of said plurality of data processorsing ~~means (IP)~~, the master ports ~~(m)~~ of the nodes ~~means (H.sub.2)~~ of the n^{th} group are coupled to said memory devicemeans ~~(SDRAM)~~, and each of the slave ports ~~(s)~~ of the nodes ~~means (H.sub.2)~~ of the n^{th} group is connected to a master port ~~(m)~~ of the nodes ~~means (H.sub.11)~~ of the $(n-1)^{th}$ group.

7. (Currently Amended) The data processing system according to claim 1, ~~characterized in that~~wherein said nodes ~~means (H.sub.11, H.sub.12, H.sub.2)~~ are hubs.

8. (Currently Amended) The data processing system according to claim 1, ~~characterized in that~~wherein said communication interface ~~means~~ further includes at least one local memory unit ~~(MEM)~~ adapted to be selectively accessed to by a memory access request.

9. (Currently Amended) The data processing system according to claim 8, ~~characterized in that~~wherein at least one node ~~means (H.sub.11, H.sub.12, H.sub.2)~~ further comprises at least one memory port ~~(mp)~~ to which a local memory unit ~~(MEM)~~ is connected.

10. (Currently Amended) The data processing system according to claim 8,

~~characterized in that~~wherein said communication interface ~~means~~ includes a cache controller ~~means~~ for controlling at least a section of the local memory unit~~(s) (MEM)~~ as a cache memory.

11. (Currently Amended) The data processing system according to claim 1, ~~characterized in that~~wherein said communication interface ~~means~~ further includes at least one synchronization means for streaming communication between data processors~~ing means (IP)~~.

12. (Currently Amended) The data processing system according to claim 11, ~~characterized in that~~wherein at least one node ~~means (H.sub.11, H.sub.12, H.sub.2)~~ includes said synchronization means for streaming communication between the data processors~~ing means (IP)~~ directly or indirectly coupled to said node~~s means~~.

13. (Currently Amended) The data processing system according to claim 11~~8~~, ~~characterized in that~~wherein the local memory unit~~(s) (MEM)~~ is ~~(are)~~ configured to provide ~~the~~ storage ~~means for~~based on a first-in/first-out function and said synchronization means comprises a first-in/first-out administration means for controlling said local memory unit~~(s) (MEM)~~.

14. (Currently Amended) The data processing system according to claim 8~~1~~, ~~characterized in that~~wherein said ~~communication interface means is provided on a single chip (C)~~memory device and said local memory unit have a single address space.

15. (Currently Amended) The data processing system according to claim 14, ~~characterized in that~~wherein at least a portion~~art~~ of said plurality of data processors~~ing means (IP)~~ is ~~additionally provided~~positioned on said single chip ~~(C)~~.